ZHEJIANG UNIU-NE Technology CO.,LTD

浙 江 宇 力 微 新 能 源 科 技 有 限 公 司

AP3065SD Data Sheet

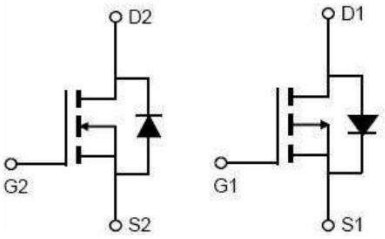
V 1.1

Feature

- **N-Channel**
  V_{DD}=40V,I_D=7A
  $R_{DS(ON)}$ <45mΩ @V_{GS}=10V TYP=30 mΩ
  $R_{DS(ON)}$ <60mΩ @V_{GS}=4.5V TYP=42 mΩ

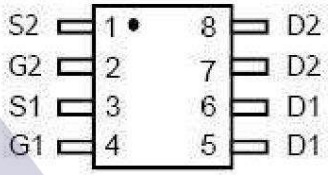
- **P-Channel**
  V_{DD}=-40V,I_D=-6A
  $R_{DS(ON)}$ <85mΩ @V_{GS}=-10V TYP=65 mΩ
  $R_{DS(ON)}$ <120mΩ @V_{GS}=-4.5V TYP=90 mΩ

- Lead free product is acquired
- High power and current handing capability
- Surface mount package



N-channel P-channel

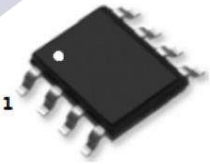
Schematic diagram



Marking and pin assignment

Application

- PWM applications
- Load Switch
- Power management



SOP-8

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
3065SD	AP3065SD	SOP-8	13 inch	-	4000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current (T_a =25℃)	I_D	7	-6	A
Continuous Drain Current (T_a =100℃)	I_D	4.9	-4.2	A
Pulsed Drain Currenr (1)	I_{DM}	28	-24	A
Power Dissipation	P_D	3	3	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	42	45	℃/W
Junction Temperature	T_J	150	150	℃
Storage Temperature	T_{STG}	-55~ +150	-55~ +150	℃

N-CH ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	40			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =40 V, V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage(2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.7	2.5	V
Drain-source on-resistance(2)	$R_{DS(on)}$	V_{GS} =10V, I_D =5A		30	45	mΩ
		V_{GS} =4.5V, I_D =3A		42	60	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =20V, V_{GS} =0V, f =1MHz		381		pF
Output Capacitance	C_{oss}			48		
Reverse Transfer Capacitance	C_{rss}			40		
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, I_D=2A, R_L=6Ω V_{GS}=10V, R_G=1Ω		4		ns
Turn-on rise time	t_r			21		
Turn-off delay time	$t_{d(off)}$			12		
Turn-off fall time	t_f			20		
Total Gate Charge	Qg	VDS=20V, ID=3A, VGS=10V		9.8		nC
Gate-Source Charge	Qgs			1.9		
Gate-Drain Charge	Qgd			2.1		
Source-Drain Diode characteristics						
Diode Forward voltage(2)	V_{DS}	V_{GS} =0V, I_S=5A			1.2	V
Diode Forward current(3)	I_S		-	-	7	A

P-CH ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-40			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-40V, V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage(2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1	-1.4	-2.5	V
Drain-source on-resistance(2)	$R_{DS(on)}$	V_{GS} =-10V, I_D =-5A		65	85	mΩ
		V_{GS} =-4.5V, I_D =-3A		90	120	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =-20V, V_{GS} =0V, f =1MHz		596		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			70		
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=-20V, I_D=-3A, R_L=6Ω V_{GS}=-10V, R_G=1Ω		9		ns
Turn-on rise time	t_r			8		
Turn-off delay time	$t_{d(off)}$			28		
Turn-off fall time	t_f			10		
Total Gate Charge	Qg	VDS=-20V, ID=-3A, VGS=-10V		14		nC
Gate-Source Charge	Qgs			2.9		
Gate-Drain Charge	Qgd			3.8		
Source-Drain Diode characteristics						
Diode Forward voltage(2)	V_{DS}	V_{GS} =0V, I_S=-5A			1.2	V
Diode Forward current(3)	I_S		-	-	-6	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. Pulse Test: pulse width≤300μs, duty cycle≤2%
3. Surface Mounted on FR4 Board,t≤10 sec

Test Circuit

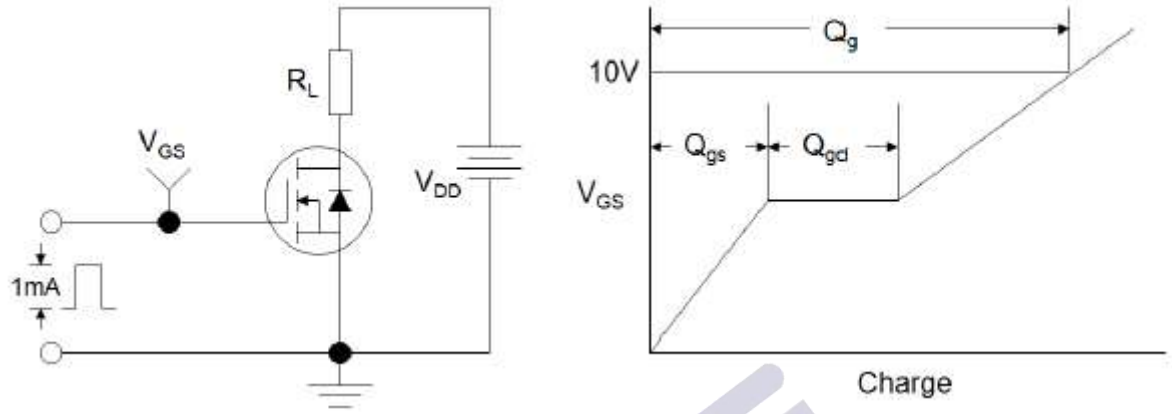


Figure1:Gate Charge Test Circuit & Waveform

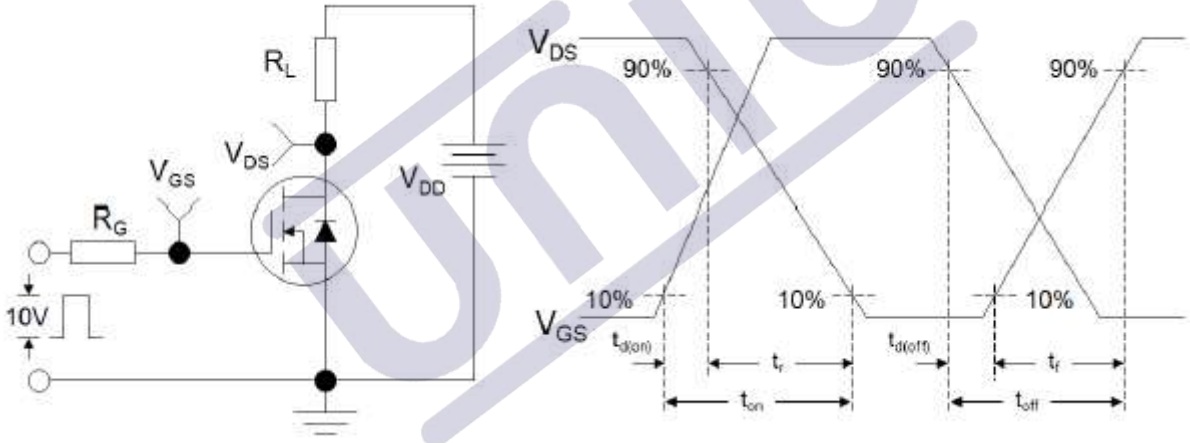


Figure 2: Resistive Switching Test Circuit & Waveforms

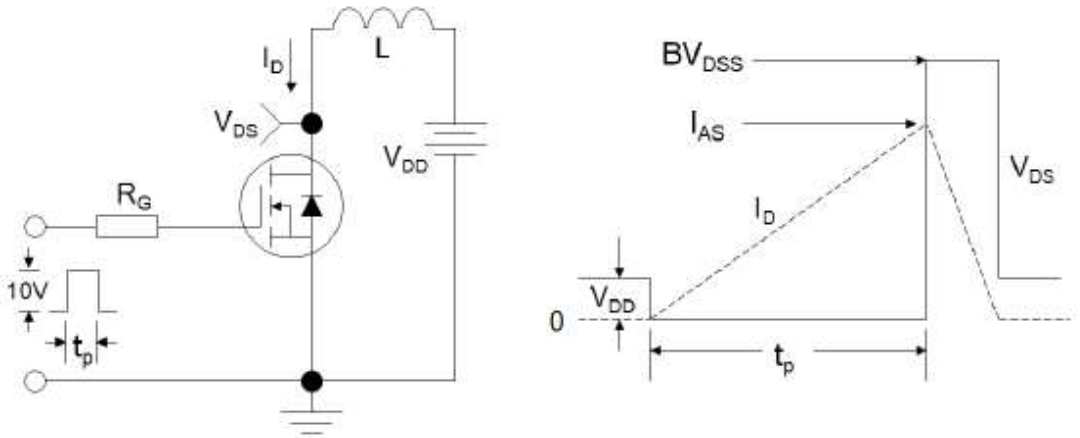


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

N-Channel

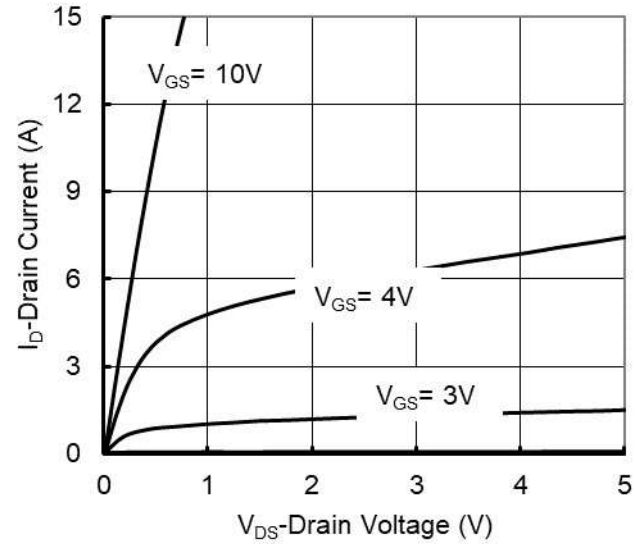


Figure1. Output Characteristics

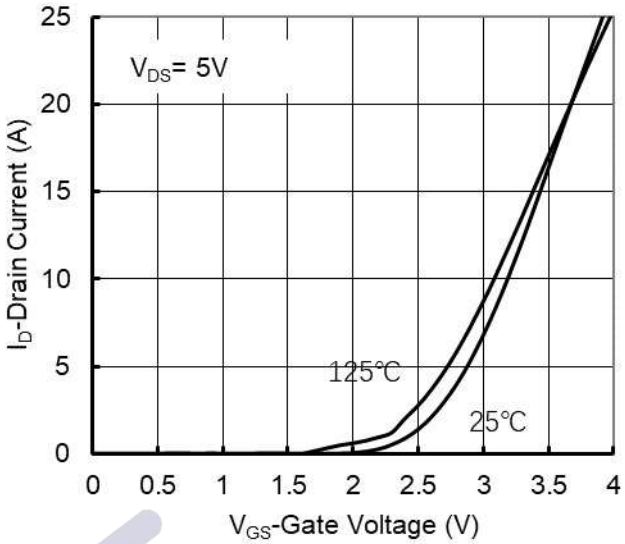


Figure2. Transfer Characteristics

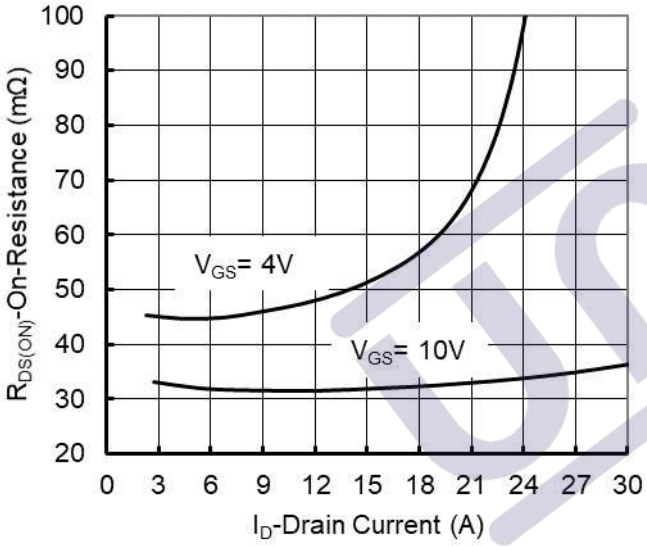


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

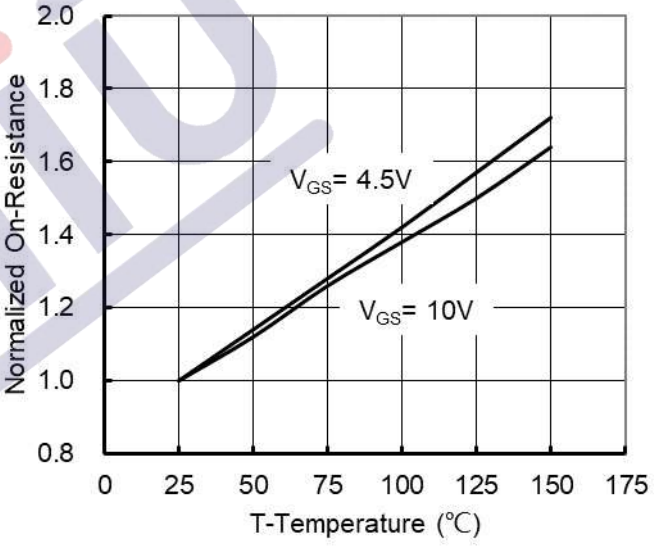


Figure 4: On-Resistance vs. Junction Temperature

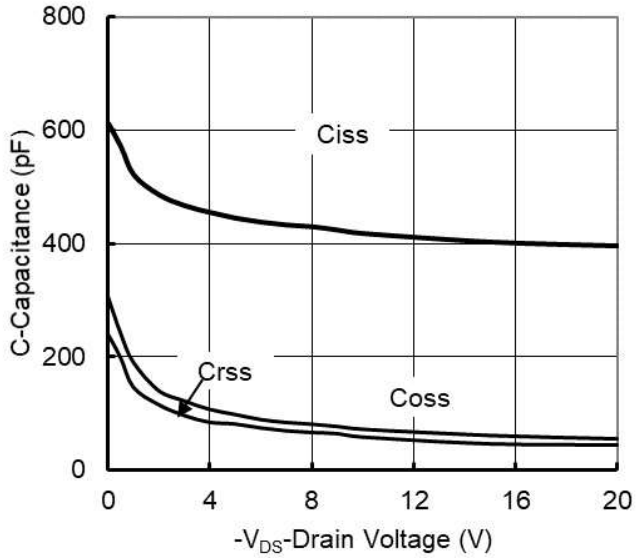


Figure5. Capacitance Characteristics

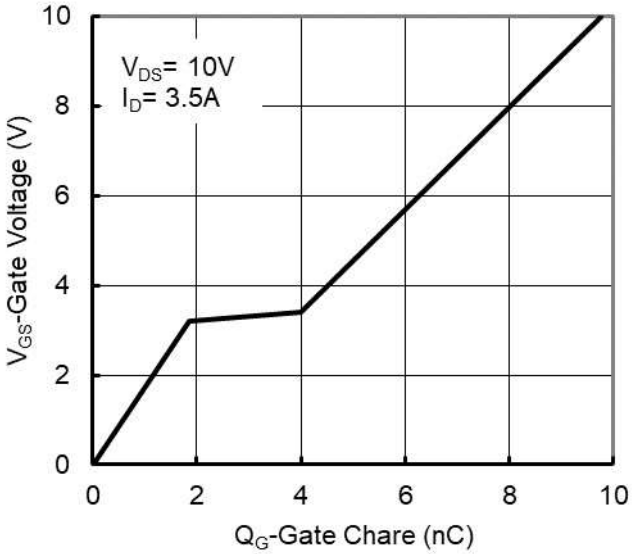


Figure6. Gate Charge

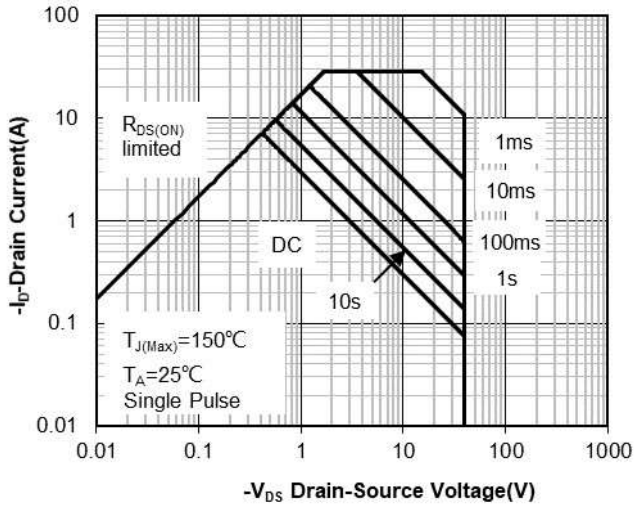


Figure7. Safe Operation Area

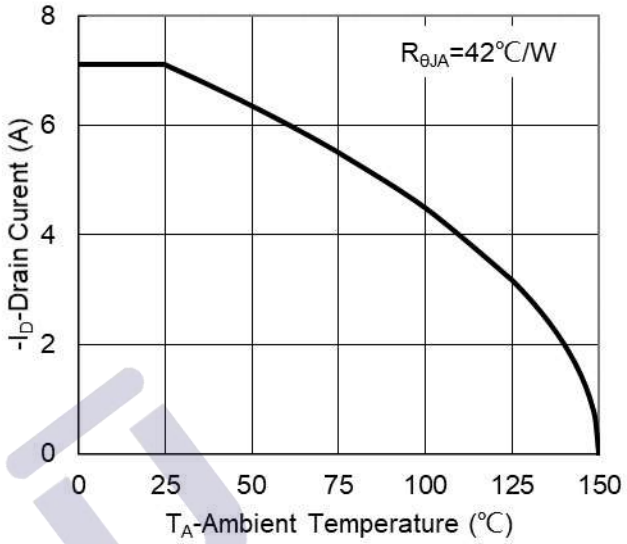


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

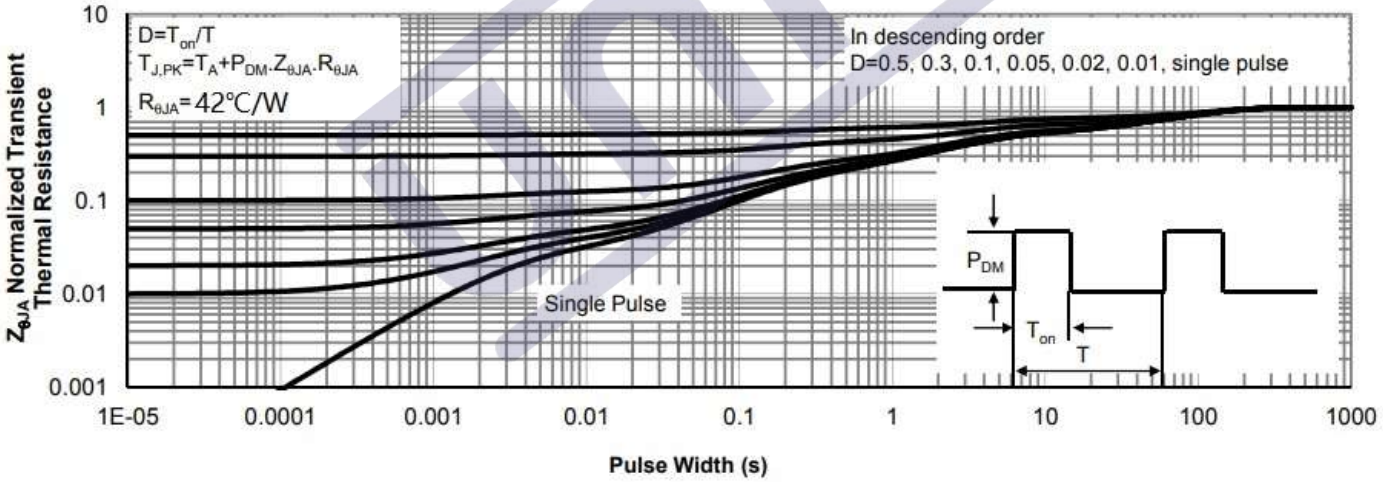


Figure9. Normalized Maximum Transient Thermal Impedance

P-Channel

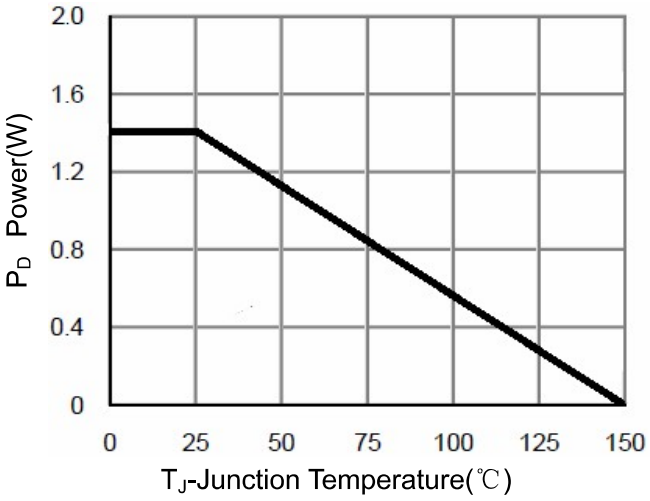


Figure 1 Power Dissipation

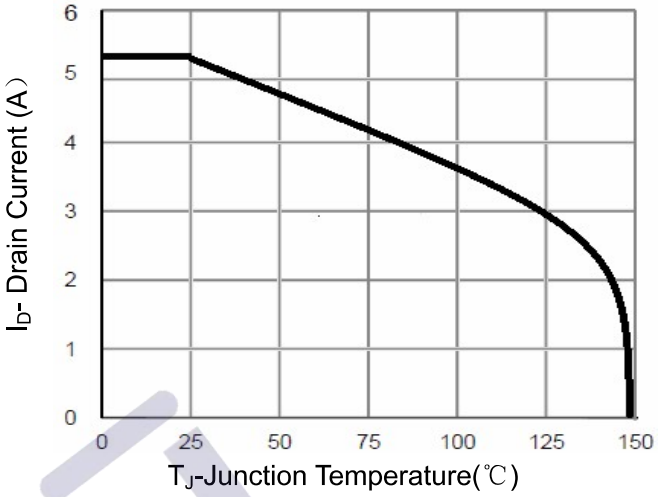


Figure 2 Drain Current

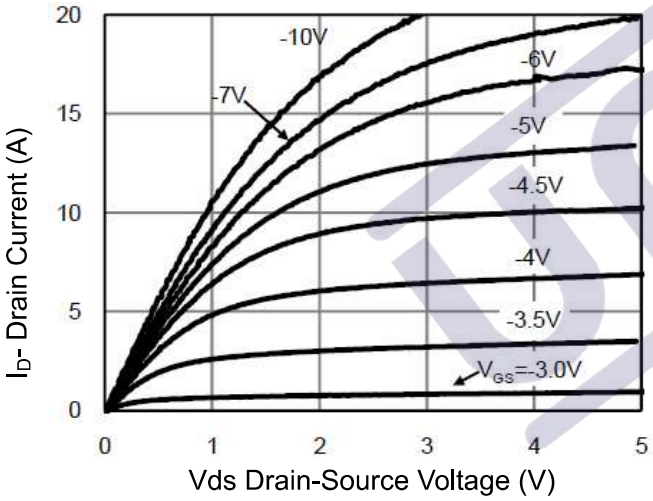


Figure 3 Output Characteristics

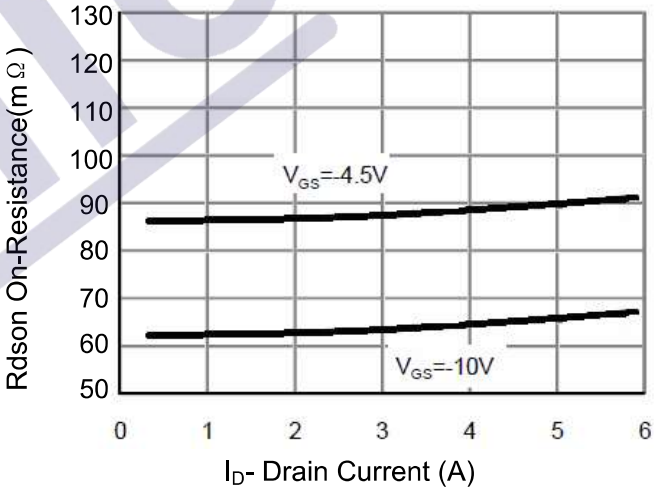


Figure 4 Drain-Source On-Resistance

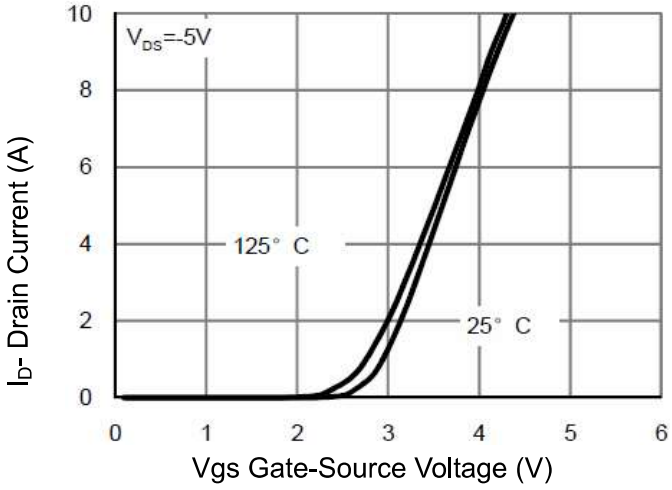


Figure 5 Transfer Characteristics

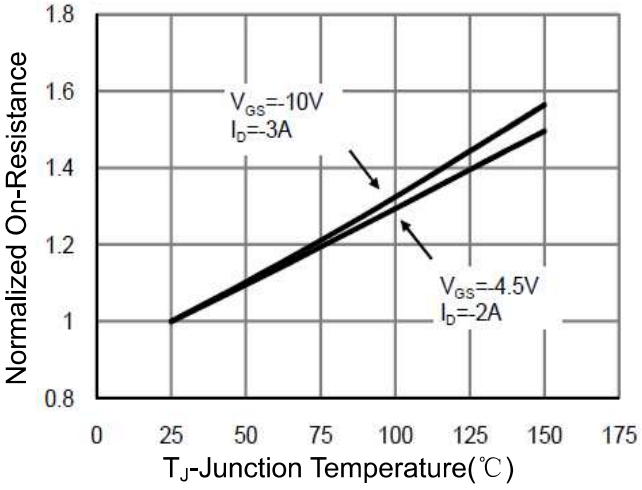


Figure 6 Drain-Source On-Resistance

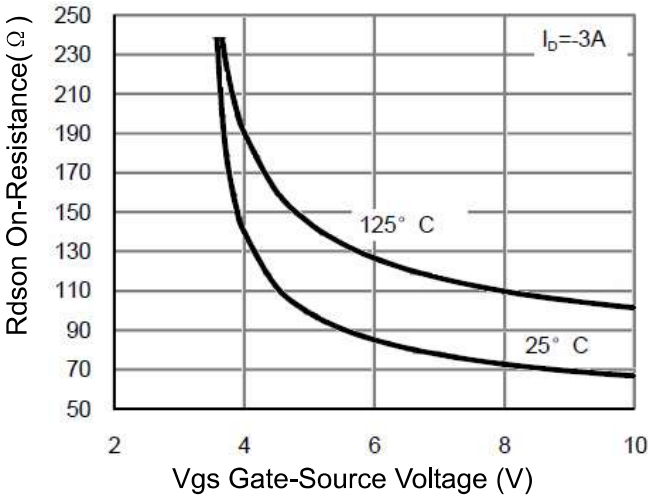


Figure 7 Rdson vs Vgs

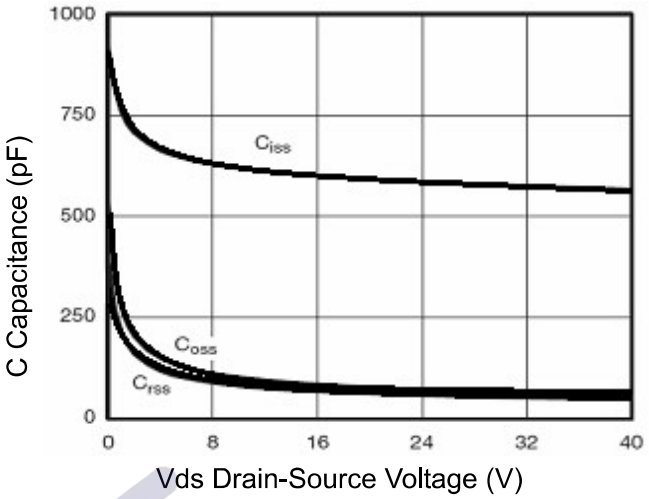


Figure 8 Capacitance vs Vds

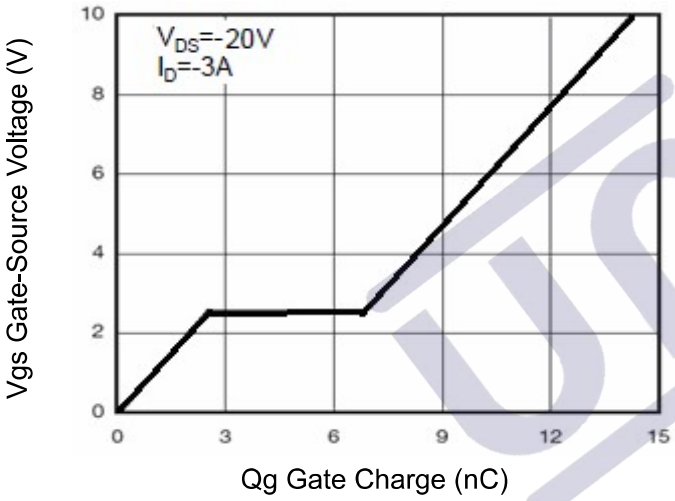


Figure 9 Gate Charge

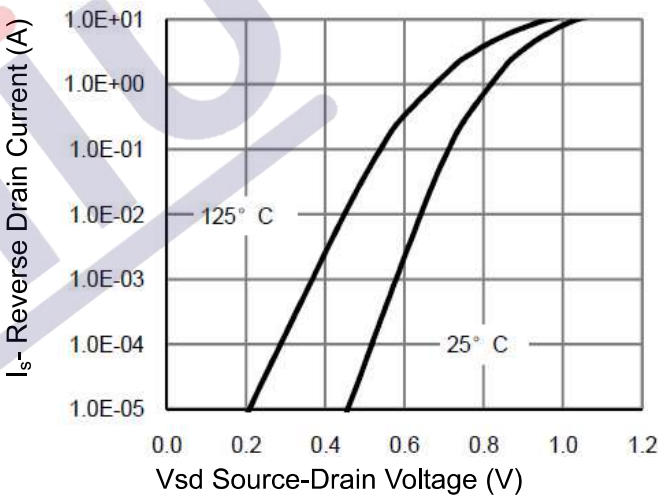


Figure 10 Source- Drain Diode Forward

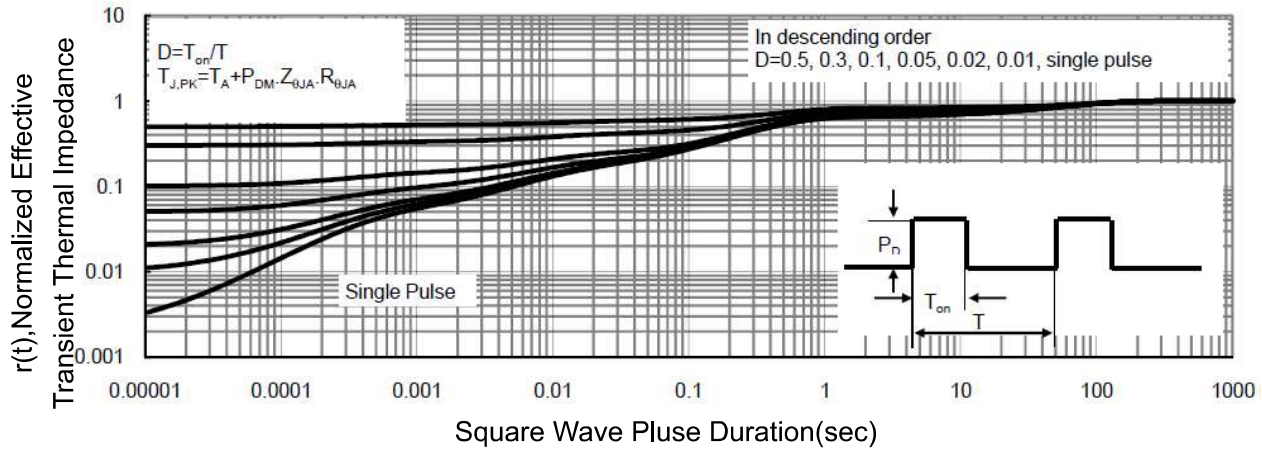


Figure 11 Normalized Maximum Transient Thermal Impedance

1.版本记录

DATE	REV.	DESCRIPTION
2021/03/19	1.0	First Release
2022/11/12	1.1	Layout adjustment

2.免责声明

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